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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/998,051 | 11/29/2001 | Andreas Wichern | DE 000214 | 5503 |

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

| EXAMINER |
|---|
| NGUYEN, LINH V |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 07/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/998,051 | WICHERN ET AL. | |
| | Examiner | Art Unit | |
| | Linh V. Nguyen | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/29/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Response to Amendment*

1. This office action is in response to applicant's amendment received on 1/11/03. Claims 1, 2, 4 and 17 have been amended. Claims 1 – 20, are pending on this application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1- 20, are rejected under 35 U.S.C. 102(e) as being anticipated by Ishihara U.S. patent No. 6,177,839.

Regarding to claims 1, and 4, Fig. 1 Ishihara discloses a variable amplifier circuit comprising: first differential amplifier stage (5, 6) having a first and a second output branch; second differential amplifier stage (9, 10, 11) that is coupled to the first output branch of the first differential amplifier stage (Collector of 5), the second differential amplifier stage having a first output branch (18) and at least a second output branch (19) for controllably dividing a first current (Io, Col. 6 lines 31 – 32) in the first output branch of the first differential amplifier stage into partial currents ( Col. 6 line 53

equation of Io); the second output branch having at least one sub-ranch that is connected to a current power supply terminal (18, 19, because 15 and 16 are current sources for differential amplifier [9, 10, 11] and [12, 13, 14], therefore terminals 18, and 19 are current supply terminals); a third differential amplifier (12, 13, 14) stage that is coupled to the second output branch of the first differential amplifier stage (Collector of 6), the third differential amplifier stage having a first output branch (19) and at least a second output branch (18) for controllably dividing a second current (Io, Col. 6 lines 31 – 32) in the second output branch of the first differential amplifier stage into partial currents ( Col. 6 line 53 equation of Io); a first load impedance (15) coupled to one of the output branches of the second differential amplifier stage for generating a first output voltage (18) from the partial current flowing in said one of the first output branches of the second differential amplifier stage; and a second load impedance (16) coupled to one of the output branches of the third differential amplifier stage for generating a second output voltage (19) from the partial current flowing in said one of the first output branches of the third differential amplifier stage; wherein the first and the second load impedance are bridged to a predetermined part by at least one of the second output branches of the second and third differential amplifier stages, respectively (11, 12).

Regarding to claim 2, wherein said one of the second output branches of the second differential amplifier stage has two jointly controlled sub-branches (9, 10), a first sub-branch of which is coupled to the first load impedance (9), and in that said one of the second output branches of the third differential amplifier stage has two jointly

controlled sub branches (13, 14), a first sub-branch (14) of which is coupled to the second load impedance.

Regarding to claim 3, wherein said one of the second output branches of the second differential amplifier stage is coupled to a tap (18) on the first load impedance, and said one of the second output branches of the third differential amplifier stage is coupled to a tap (19) on the second load impedance.

Regarding to claim 5, wherein the variable amplifier comprising at least two controllable amplifier arrangements (5, 6, and 9 – 14), wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals (1 – 4) and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals,

Regarding to claim 6, wherein the output branches of the second and the third differential amplifier stage are formed with transistors whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at the different values of the common control signals in the individual controllable amplifier arrangements (Fig. 2, See Col. 5 line 66 to Col. 6 line 8).

Regarding to claim 7, wherein the first amplifier differential stage comprises a plurality of bipolar transistors (Fig. 2).

Regarding to claim 8, wherein the second amplifier differential stage comprises a plurality of bipolar transistors (Fig. 2).

Regarding to claim 9, wherein the first load impedance is an ohmic resistor (15).

Regarding to claim 10, wherein said one of the second output branches of the second differential amplifier stage has two jointly controlled sub-branches (9, 10), a first sub-branch (9) of which is coupled to the first load impedance (15), and in that said one of the second output branches of the third differential amplifier stage has two jointly controlled sub-branches (13, 14), a first sub-branch (14) of which is coupled to the second load impedance (16).

Regarding to claim 11, Fig. 2 Ishihara disclose the arrangement for variable gain amplifier circuit comprising at least two controllable amplifier arrangements (5, 6 and 9 – 14), wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals (1, 2) and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of common control signal (1, 2).

Regarding to claim 12, wherein the output branches of the second and the third differential amplifier stage are formed with transistor whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at different values of the

common control signals in the individual controllable amplifier arrangements (See Col. 5 line 66 to Col. 6 line 8).

Regarding to claim 13, wherein said one of the second output branches of the second differential amplifier stage is coupled to a tap (18) on the first load impedance, and said one of the second output braches of the third differential amplifier stage is coupled to a tap (19) on the second load impedance.

Regarding to claim 14, the variable gain amplifier comprising at least two controllable amplifier arrangements (5, 6, and 9 –14), wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals (1, 2) and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals (Fig. 2).

Regarding to claim 15, wherein the output branches of the second and the third differential amplifier stage are formed with transistors whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at the different values of the common control signals in the individual controllable amplifier arrangements (Fig. 2, See Col. 5 line 66 to Col. 6 line 8).

Regarding to claim 16, wherein the first differential amplifier stage comprises a plurality of bipolar transistors (Fig. 2).

Regarding to claim 17, Fig. 2 Ishihara discloses a controllable amplifier, comprising: a first-stage differential amplifier (5, 6) having a first and a second output branch; a second-stage differential amplifier coupled to the first first-stage output branch, the second-stage differential amplifier (9, 10, 11) having a first and a second output branch for controllably dividing a first current (Io) in the first first-stage output into partial currents; a third-stage differential amplifier (12, 13, 14) coupled to the second first-stage output branch, the third-stage differential amplifier having a first and a second output branch for controllably dividing a first current (Io) in the second first-stage output into partial currents; a first second-stage impedance load (15) coupled to the first second-stage output branch; a second second-stage impedance load (16) coupled to the first second-stage impedance load and to the second second-stage output branch (11), and connected to a current power supply terminal (18, 19, because the resistor load 15 and 16 of Ishihara are the current sources for differential amplifier [12, 13, 14] and [9, 10, 11] therefore 18 or 19 are current supply output terminals of 15 and 16), the first and second second-stage impedance loads for generating a first output voltage at an output tap (18) coupled between them; a first third-stage impedance load (18) coupled to the first third-stage output branch (14); and a second third-stage impedance load (15) coupled to the first third-stage impedance load and to the second third-stage output branch (12), and connected to a current power supply terminal (18, 19, because the resistor load 15 and 16 of Ishihara are the current sources for differential amplifier

[12, 13, 14] and [9, 10, 11] therefore 18 or 19 are current supply output terminals of 15 and 16), the first and second third-stage impedance loads for generating a second output voltage at an output tap coupled between them (19); wherein the first output branches of the first-stage and the second-stage differential amplifiers are each coupled to be controlled by a first control voltage (1, 2, 3), and wherein the second output branches of the first-stage and the second-stage differential amplifiers are each coupled to be controlled by a second control voltage (4, 1, 2).

Regarding to claim 18, wherein the first second stage impedance load is an ohmic resistor (15, 16).

Regarding to claim 19, wherein the first-stage differential amplifier comprises a plurality of bipolar transistors (Fig. 2).

Regarding to claim 20, wherein the second- stage differential amplifier comprises a plurality of bipolar transistors (Fig. 2).

***Response to Arguments***

Applicant's arguments filed 6/16/03 with respect to amended claims 1, 4, and 17, have been fully considered but they are not persuasive, because in Ishihara's Figure 2, the 15 and 16 elements are providing current supply to differential amplifiers.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

July 14, 2003.

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800